Exhibit 3

Paper No. __

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

GOOGLE LLC,
Petitioner,

v.

SINGULAR COMPUTING LLC,
Patent Owner.

_____

Case No. IPR2021-00178
Patent No. 8,407,273

_____

PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq

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1050	Katherine Bourzac, *The First Carbon Nanotube Computer*, MIT Technology Review, Sep. 25, 2013 (accessed Sep. 8, 2020) ("Bourzac")
1051	Joe Touch et. al,, *Optical Computing*, Nanophotonics 2017 6(3): 503-505 ("Touch")
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MANDATORY NOTICES

A. Real Party-In-Interest

Petitioner is the Real Party-in-Interest.

B. Related Matters

A decision in this proceeding could affect or be affected by the following:

1. United States Patent & Trademark Office

The application from which U.S. Patent No. 8,407,273 ("the '273 patent") issued is a Continuation of U.S. Patent Application No. 12/816,201 (U.S. Patent No. 8,150,902), which claims Priority to U.S. Provisional Application No. 61/218,691.

The following U.S. patent applications also claim the benefit of the priority of the filing date of U.S. Provisional Application No. 61/218,691:

13/849,606; 14/976,852; 15/784,359; 16/175,131; 16/571,871; 16/675,693; 16/882,686; 16/882,694; and 17/029,780.

2. United States Patent Trial and Appeal Board

Concurrently with the present Petition, Petitioner is filing a second petition challenging claims 1-26, 28, 32-61, 63, and 67-70 of the '273 patent. Petitioner requests that these two petitions challenging the '273 patent be reviewed by the same panel.

Petitioner also previously filed petitions for *inter partes* review of related U.S. Patents Nos. 9,218,156 (under case nos. IPR2021-00164 and IPR2021-00165) and 10,416,961 (under case nos. IPR2021-00154 and IPR2021-00155). Petitioner

requests that these additional petitions also be reviewed by the same panel as the present Petition, as the patents are commonly assigned and share the same specification, and there are numerous overlapping elements among the claims of all three patents.

3. U.S. District Court for the District of Massachusetts

Singular Computing LLC v. Google LLC, Case No. 1:19-cv-12551-FDS.

C. Counsel and Service Information - §§ 42.8(b)(3) and (4)

Lead Counsel	Elisabeth H. Hunt, Reg. No. 67,336
Backup Counsel	Richard F. Giunta, Reg. No. 36,149 Anant K. Saraswat, Reg. No. 76,050 Nathan R. Speed (*pro hac vice* forthcoming)
Service Information	E-mail: EHunt-PTAB@wolfgreenfield.com Rgiunta-PTAB@wolfgreenfield.com ASaraswat-PTAB@wolfgreenfield.com nspeed@wolfgreenfield.com Post and hand delivery: Wolf, Greenfield & Sacks, P.C. 600 Atlantic Avenue Boston, MA 02210-2206 Telephone: 617-646-8000 Facsimile: 617-646-8646

A power of attorney is submitted with the petition. Counsel for Petitioner consents to service of all documents via electronic mail.

Petitioner requests *inter partes* review and cancellation of claims 1-70 ("challenged claims") of the '273 patent (Ex. 1001).

I. INTRODUCTION

The '273 patent claims a device comprising at least one "low precision high dynamic range (LPHDR) execution unit." The claimed "execution unit" is adapted to execute an operation (*e.g.*, multiplication) on an input signal representing a first numerical value to produce an output signal representing a second numerical value. The "execution unit" is characterized as "LPHDR" because it performs a low precision ("LP") operation on a high dynamic range ("HDR") of values. Goodin Declaration (Ex. 1003, "Goodin"), ¶ 20.

A "low precision arithmetic" operation, the '273 patent says, is less precise than an exact calculation, such that "each operation might introduce" some "error" in its "results." '273 patent, 4:9-12; Goodin, ¶ 23. For example, a low-precision operation may produce a result of 2.1 when the exact operation would produce a result of 2.13. "Dynamic range" refers to the range of numerical values supported. '273 patent, 2:35-39; Goodin, ¶ 24. For example, a signal that can represent any numerical value between 1 and 100 has a higher dynamic range than one that can only represent numerical values between 1 and 10.

Claim 1's "execution unit" operates on a dynamic range of possible valid inputs "at least as wide as from 1/65,000 through 65,000," and for some minimum

claimed percentage of the possible inputs (*i.e.*, at least 5%), the outputs the execution unit generates differ on average by a claimed minimum amount (*i.e.*, at least 0.05%) from the result of an "exact mathematical calculation" of that operation on "the numerical values" of those "same input[s]."

Petitioner's concurrently filed petition demonstrates that claim 1 and other claims are rendered unpatentable by multiple references that described LPHDR execution units before the '273 patent's earliest claimed priority date. This petition, however, demonstrates that the challenged claims are also unpatentable over the inventor's own published priority application because no challenged claim is entitled to the earlier filing date of that priority application, which is indisputable prior art because it published more than a year earlier than any priority date to which any challenged claim is entitled.

To be entitled to an earlier application's filing date, a challenged claim must be "disclosed" in that earlier application "in the manner provided by section 112(a)," 35 U.S.C. § 120, meaning it must find written description support in, and be enabled by, the disclosure of the earlier application(s). The '273 patent purports to claim priority to earlier-filed application 12/816,201 ("'201 Application," Ex. 1005), but that application (which shares the '273 patent's specification) does not provide written description of, or enabling disclosure for the full scope of, any challenged claim.

As discussed in Ground 1, the challenged claims cover a genus of "execution units" defined by a functional performance characteristic. The execution unit must be adapted to execute a first operation (which can include ***any*** mathematical operation) on a high dynamic range of values, and produce an output signal that meets specified imprecision characteristics, *i.e.*, the result must differ by a specified amount from the exact mathematical calculation of the operation on the same input values for a specified percentage of the possible valid inputs within the dynamic range. The claimed "execution units" are limited not by what they are, but by what they do—execute an operation with the specified degree of imprecision. Goodin, ¶ 37.

As for what the specification says the "execution units" ***are***, the inventor (Dr. Joseph Bates) was clear that the claims cover ***any*** implementation of an "execution unit" that happens to possess the claimed functional performance characteristics. The specification discusses an execution unit embodiment implemented—like most modern computing processors—using silicon transistors, but is explicit that "silicon chip fabrication technology…does not constitute a limitation of the present invention." '273 patent, 26:17-20. The claimed "present invention" also covers implementations using non-conventional technologies:

> includ[ing] various nanomechanical and nanoelectronic technologies, chemistry based technologies such as for DNA computing, nanowire and nanotube based technologies, optical technologies, mechanical

> technologies, biological technologies, ***and other technologies*** whether based on transistors or not that are capable of implementing LPHDR architectures of the kinds disclosed herein.

Id., 26:17-31.[1]

At least some of these listed technologies were—at best—nascent and unpredictable in 2010 when the '201 Application was filed. Yet, the specification does nothing more than allege that those technologies "***may*** enable other sorts of traditional digital and analog computing processors." *Id.*, 26:22-24. Dr. Bates did not describe an "execution unit" he possessed that was implemented using any of these listed technologies. The reason for his silence is simple—he could not describe what he had not invented.

Making that silence even more problematic, the specification is clear that the claims cover not only ***any*** implementation of an "execution unit" that performs ***any*** operation using ***any*** technology (*e.g.*, DNA, nanomechanical, etc.), but also any implementation that operates on digital representations of numbers, analog representations of numbers, or both. Dr. Bates claimed the use of all LPHDR "execution units," including not only a conventional silicon transistor-implemented unit executing operations on conventional digital representations of numbers like floating-point representations, but also DNA, nanomechanical, and "other

[1] Emphasis is added throughout.

technologies"-implemented execution units executing operations on ***analog*** representations of numbers where numerical values are represented by "charges, currents, voltages,…various forms of spikes or in ***other [unstated] forms*** not characteristic of traditional digital implementations." *Id.*, 14:16-21. Yet, even seven years after he filed the '201 Application, Dr. Bates admitted publicly that "I couldn't figure out how to do it in analog." Ex. 1022, 5:6-13.

The '273 patent's specification includes an aspirational wish-list of technologies that "may enable other sorts of traditional digital and analog computing processors or other devices" beyond traditional silicon-implemented processors, and alleges that these technologies could be used in some undescribed way to implement a high dynamic range execution unit that meets the claimed imprecision functional performance characteristics. '273 patent, 26:17-24; Goodin, ¶ 37. But claiming all execution units "that achieve a result without defining what means will do so is not in compliance with [section 112's] description requirement; it is an attempt to preempt the future before it has arrived." *Fiers v. Revel*, 984 F.2d 1164, 1171 (Fed. Cir. 1993).

Unsurprisingly, given the aspirational nature of many "implementations" the specification explicitly says the claims cover, the '201 Application—which shares an identical specification with the '273 patent and to which the '273 patent claims priority—neither demonstrates possession of nor enables the full scope of any

challenged claim. As a result, Bates-2010—the version of the '201 Application published in 2010—is indisputable prior art.

As explained *infra* § V.D, Bates-2010 renders the challenged claims obvious because it mentions an implementation that uses conventional silicon transistor-based digital circuitry. Petitioner relies on obviousness rather than anticipation because although Bates-2010's specification discusses this implementation and separately lists desired functional performance characteristics that an execution unit implemented using ***any*** of the listed technologies allegedly could somehow be made to possess, the specification never ties the two together in a manner that demonstrates possession of an execution unit that is implemented using silicon transistor-based digital circuitry exhibiting the claimed functional performance characteristics. Stated differently, the specification does not describe the implementation techniques that would ensure that an execution unit implemented using silicon transistor-based digital circuitry would possess the specific functional performance characteristics required for any challenged claim. Despite that, it would have been obvious to a POSA how to fill in the gaps the specification leaves for an execution unit using silicon transistor-based digital circuitry, to arrive at a species of execution unit that would meet the claimed performance characteristics, which Bates-2010 explicitly identifies as desirable. *Infra* § V.D; *Ariad Pharms. Inc., v. Eli Lilly & Co.*, 598 F.3d

1336, 1352 (Fed. Cir. 2010) ("[A] description that merely renders the invention obvious does not satisfy [written description].").

While Bates-2010 does not support the ***full*** scope of any challenged claim, it need not do so to render the claim unpatentable, as rendering obvious even a single species within a claimed genus renders the genus claim unpatentable. *Ex Parte Kubin*, 2007 WL 2070495, *4 (B.P.A.I. 2007) (precedential) ("A single, obvious species within a claimed genus renders the claimed genus unpatentable under § 103."), *affirmed by* 561 F.3d 1351 (Fed. Cir. 2009). The Federal Circuit and Board have often found a claim invalidated by a parent patent having the same disclosure where, as here, the patentee improperly claims a much broader invention than was disclosed and/or enabled. *Infra* § V.D.2.

II. GROUNDS FOR STANDING

Petitioner certifies the '273 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the challenged claims. 37 C.F.R. § 42.104(a).

III. GROUNDS OF UNPATENTABILITY

The challenged claims would have been obvious under section 103 in view of Bates-2010, which is prior art under pre-AIA section 102(b).

Ground Number and Reference(s)		Claims
1	Bates-2010 (Ex. 1006)	1-70

IV. THE '273 PATENT

A. Independent Claims

The '273 patent includes independent claims 1, 33, 36 and 68. Claim 1 (reproduced below with claim elements annotated) is illustrative.

> [1A1] A device comprising: at least one first low precision high dynamic range (LPHDR) execution unit
>
> [1A2] adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,
>
> [1B1] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000 and
>
> [1B2] for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.

[1A1]-[1A2] recite a device comprising an LPHDR execution unit adapted to execute an operation. [1B1] recites a claimed dynamic range of the inputs, and [1B2] recites a claimed minimum imprecision of the operation in terms of minimum relative error (Y) produced for a minimum percentage (X) of inputs. Goodin, ¶ 38.

Independent claim 36 recites the identical device as claim 1 but introduces a "wherein" clause requiring that the number of LPHDR execution units "exceeds the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide."

Independent claim 33 recites a "device comprising a computer processor and a computer-readable medium storing computer program instructions, wherein the computer program instructions are executable by the processor to emulate a second device" identical to claim 1's device. Independent claim 68 is similar except the emulated "second device" is identical to claim 36's device.

B. Person of Ordinary Skill in the Art ("POSA")

The timeframe for evaluating written description and enablement in the '201 Application is 2010 when that application was filed. *Infra* § V.B.1. A POSA in 2010 would have had at least a bachelor's degree in Electrical or Computer Engineering, Applied Mathematics, or the equivalent, and at least two years of academic or industry experience in computer architecture. Goodin, ¶¶ 43-44. More education could substitute for less experience, and vice versa. *Id.*

Petitioner believes the timeframe for evaluating obviousness of the claims over Bates-2010 is February 17, 2012, the '273 patent's actual filing date. However, to simplify this proceeding, the level of skill applied in evaluating obviousness of

the challenged claims over Bates-2010 is the same 2010 level of skill used in demonstrating a lack of support in the '201 Application. Goodin, ¶¶ 42, 45. Demonstrating that the claims would have been obvious in 2010 demonstrates that they remained obvious any time in the future as POSAs' level of skill only increases over time.

C. Claim Construction

Claim terms are construed herein using the *Phillips* standard. 37 C.F.R. § 42.100(b). Bates-2010's disclosure is identical to the '273 patent's disclosure. Because this common disclosure is the context in which the challenged claims would be construed under *Phillips* and because it provides verbatim disclosure for most terms in the challenged claims, the Board need not expressly construe any term. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

D. Prosecution History

The examiner allowed the challenged claims, and the parent application's claims, without substantively discussing any prior art. Ex. 1042, 165-66; Ex. 1002, 164-67.

V. GROUND 1: BATES-2010 RENDERS OBVIOUS CLAIMS 1-70

A. Bates-2010 Is Prior Art Because the Challenged Claims Are Not Entitled to the '201 Application's Priority Date

The '273 patent claims priority to the 2010 filing date of the '201 Application. '273 patent, (63). The '273 patent's claims "are not entitled to [that] earlier priority date merely because the patentee claims priority." *In re NTP, Inc.*, 654 F.3d 1268, 1276 (Fed. Cir. 2011). Instead, the claims must be "disclosed" in the '201 Application "in the manner provided by section 112(a)" to be entitled to the earlier date. 35 U.S.C. § 120. The '201 Application thus must (1) provide written description demonstrating "the patentee had ***possession*** of the claimed invention at the time of the application, *i.e.*, that the patentee invented what is claimed," and (2) "enable [a POSA] to practice the ***full*** scope of the claimed invention." *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345-46 (Fed. Cir. 2005).

Petitioner has the initial burden of demonstrating that Bates-2010 is prior art, and satisfied that burden by showing that Bates-2010's publication date precedes the '273 patent's filing date of February 17, 2012. Bates-2010, (43); *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1379 (Fed. Cir. 2015) (burden of production satisfied by "arguing" reference was prior art); *Unified Patents Inc. v. Am. Patents, LLC*, IPR2019-00482, Paper 115, 15 (Aug. 13, 2020). Petitioner has done far more and has identified extensive claimed subject matter the '201 Application does not enable or demonstrate that the inventor possessed.

If Patent Owner ("Singular") argues Bates-2010 is not prior art to any challenged claim(s), Singular has the burden of producing evidence and argument establishing that each such challenged claim has written description support in ***and*** is enabled by the '201 Application. *Dynamic Drinkware,* 800 F.3d at 1379-80; *Technology Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327-28 (Fed. Cir. 2008). Although Petitioner bears the ultimate burden of persuasion, if Singular fails to meet its burden of production for any challenged claim, that claim is not entitled to the earlier '201 Application's filing date. *Unified Patents*, IPR2019-00482, Paper 115, 15-16; *Intel Corp. v. Daniel L. Flamm*, IPR2017-00279, Paper 31, 14-15 (Sept. 30, 2020).

The disclosures in the '273 patent, '201 Application, and Bates-2010 are substantively identical other than their originally filed claims. Goodin, ¶ 48. Below, citations are made to the '273 patent when explaining the challenged claims' scope (*infra* § V.B.2), to the '201 Application when addressing whether it supports the challenged claims (*infra* §§ V.B.3, V.C.2-V.C.3), and to Bates-2010 when addressing how its disclosure renders the challenged claims unpatentable (*infra* § V.D).

B. Written Description: The '201 Application Does Not Demonstrate Possession of Any Challenged Claim

1. Written Description Requires Demonstrating Full Possession of the Invention

Written description requires an applicant, like Dr. Bates, to demonstrate he "was in ***full*** possession of the claimed subject matter on the application filing date." *TurboCare v. Gen. Elec. Co.*, 264 F.3d 1111, 1118 (Fed. Cir. 2001). The specification must provide sufficient description to show the inventor actually invented what is claimed—a "mere wish or plan for obtaining the claimed invention" is not enough. *Centocor Ortho Biotech, Inc. v. Abbott Labs.*, 636 F.3d 1341, 1348 (Fed. Cir. 2011).

As explained below, the '201 Application fails to describe (or enable) any challenged claim's full scope because each claim encompasses subject matter Dr. Bates did not invent. The Federal Circuit's *LizardTech* decision provides a helpful analogy:

> "[S]uppose that an inventor created a particular fuel-efficient automobile engine and described the engine in such detail in the specification that a person of ordinary skill in the art would be able to build the engine. Although the specification would meet the requirements of section 112 with respect to a claim directed to that particular engine, it would not necessarily support a broad claim to every possible type of fuel-efficient engine, no matter how different in structure or operation from the inventor's engine."

424 F.3d at 1346.

Dr. Bates did what *LizardTech* warned against. As discussed *infra* § V.B.3.a, the only implementation the '201 Application describes in any level of detail is a digital execution unit implemented using silicon transistors (analogous to *LizardTech's* automobile engine).[2] But the challenged claims' scope encompasses ***all*** HDR execution units having the claimed low-precision functional performance characteristics (analogous to *LizardTech*'s "fuel-efficient" functional performance characteristic), "no matter how different in structure or operation" those units are from a silicon transistor-based digital execution unit. *Id*.

Functionally defined genus claims, like *LizardTech*'s hypothetical claims and Singular's challenged claims, "can be inherently vulnerable" to written description failures "especially in technology fields that are highly unpredictable, where it is difficult to establish a correlation between structure and function for the ***whole*** genus or to predict what would be covered by the functionally claimed genus." *AbbVie*

[2] The '201 Application does not even demonstrate possession of that implementation (*infra* § V.B.3.a), but a POSA would have known how to modify what is disclosed to implement, for simple arithmetic operations, an "execution unit" using silicon transistors in a manner meeting the claimed low-precision functional performance characteristics.

Deutschland GmbH & Co., KG v. Janssen Biotech, Inc., 759 F.3d 1285, 1301 (Fed. Cir. 2014) (specification failed to support "the ***full*** scope" of claims that claimed "every fully human IL-12 antibody that would achieve a desired result").[3] Although computer engineering may be a predictable art when conventional silicon transistors and digital representations of numbers are used, the '273 specification is explicit that the claims cover "execution units" implemented using technology in indisputably unpredictable fields (*e.g.*, DNA computing, nanomechanical) and using analog and/or "other" unidentified representations of numbers that introduce further unpredictability. *Infra* § V.B.2 (discussing challenged claims' breadth). Singular's functionally defined genus claims are "inherently vulnerable" for the reasons *AbbVie* recognized.

Finally, that the '201 Application mentions various implementation technologies (discussed *infra* § V.B.3.b(2)) and alleges they "may" (in some unstated way) be used to implement "execution units" with the claimed functional performance characteristics does not satisfy the written description requirement. As the *en banc* Federal Circuit explained in *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598

[3] *See also Billups-Rothenberg, Inc. v. Associated Reg. and Univ. Pathologists, Inc.*, 642 F.3d 1031, 1037 (Fed. Cir. 2011); *Pernix Ireland Pain DAC v. Alvogen Malta Ops. Ltd.*, 323 F. Supp. 3d 566, 619 (D. Del. 2018) (Bryson, J.).

F.3d 1336, 1349 (Fed. Cir. 2010), even claim language appearing ***verbatim*** in a priority application does not provide written description support for "genus claims that use functional language to define the boundaries of a claimed genus. In such a case, the functional claim may simply claim a desired result, and may do so without describing species that achieve that result." As explained *infra* § V.B.3, to support the challenged claims' genus of execution units, the '201 Application would need to demonstrate possession of the genus by describing either a number of species representative of the ***entire*** genus, or structural features common to the genus of execution units that meet the claimed imprecision performance characteristics. The '201 Application does neither.

2. The Challenged Claims Broadly Cover a Genus of "Execution Units" Defined by Its Functional Performance

To assess whether the challenged claims reach beyond subject matter Dr. Bates possessed in 2010, the challenged claims' scope must be understood. As discussed below, the claims recite a broad genus defined not by its structure but by its functional performance.

a. The Claims Recite Any "Execution Unit" Adapted to Execute Any "Operation"

Each challenged claim recites an "execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value." The patent does not define

"execution unit" or tie it to any particular structure; rather, the "execution unit" is characterized by what it does (execute an operation on an HDR input) and how accurately it does it (with low precision). Goodin, ¶¶ 49-51.

The '273 specification says an "execution unit" can be implemented using digital circuits that operate on digital representations (using binary 0s and 1s) of numerical values (*e.g.*, 11:53-56)[4], analog circuits operating on analog representations of numerical values (*e.g.*, 14:16-26), or combinations of the two (24:47-57). Goodin, ¶¶ 52-53. The specification describes numerous types of number representations, including but not limited to (*i.e.*, "such as"), "fixed point, logarithmic, or floating point" digital representations (24:49-50) and analog representations taking the form of "charges, currents, voltages, frequencies, pulse widths, pulse densities, various forms of spikes, or in ***other forms*** not characteristic of traditional digital implementations" (14:16-26; 24:50-53). These "representations may be used individually ***or in combination***." 24:50-53.

While certain embodiments may be implemented using transistors and "silicon chip fabrication technology," "this is merely an example and does not constitute a limitation of the present invention." 26:17-20. Instead, "the present invention may be implemented using technologies that ***may enable*** other sorts of

[4] Citations in § V.B.2 are to Ex. 1001 unless otherwise specified.

traditional digital and analog computing processors" such as "various nanomechanical and nanoelectronic technologies," or "chemistry based technologies such as for [sic] DNA computing" or "nanowire and nanotube based technologies,…and ***other [unstated] technologies whether based on transistors or not*** that are capable of implementing LPHDR architectures." 26:17-31; Goodin, ¶ 54.

Independent claim 6 of related U.S. Patent No. 10,416,961 makes explicit that the generic "execution unit" in the claims encompasses these technologies, as that claim has a wherein clause narrowing the earlier-recited generic "execution unit" to comprise one of a: chemistry-technology-based, biological-technology-based, DNA-technology-based, nanomechanical-technology-based, nanoelectronic-technology-based, nanowire-technology-based, nanotube-technology-based, and optical-technology-based execution unit. '961 Patent (Ex. 1061), 31:1-13; *see also* U.S. Patent No. 9,218,156 (Ex. 1062), 30:44-53, 31:59-32:4; *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003) ("[S]ame claim term in…related patents [presumptively] carries the same construed meaning.").

Similarly, the "operation" the execution unit performs ranges from "addition, multiplication, subtraction, and division" ('273 Patent, 11:44-48) to "trigonometric functions" (27:33-39) and even "non-linear operations such as exponentiation" (1:64-66). Goodin, ¶ 55.

Additionally, the claims expressly cover ***non-deterministic*** implementations, *i.e.*, execution units that produce different results for different executions of the same operation on the same input. Goodin, ¶ 56. All challenged claims recite "repeated execution" of the operation on "that same input" and taking a "statistical mean" (average) of the output numerical values. *See* claims 1, 33, 36 and 68. The specification says some embodiments (*e.g.*, analog embodiments) are non-deterministic (4:7-13, 14:16-26), and even says some digital embodiments "may not yield deterministic…results" (26:42-46). The claims expressly cover these non-deterministic embodiments via the recited "statistical mean" provisions. Goodin, ¶¶ 56-60.

As shown above, the '273 patent is clear that the claimed "execution unit" covers a dizzying array of potential implementations. According to the patent, each "execution unit" implementation must involve at least one selection from each of the at least three classes of variables identified below (Goodin, ¶¶ 61-64):

1. **Implementing Technology**. Each "execution unit" is implemented using one of nine identified technologies ("silicon," "nanomechanical," "nanoelectrical," "DNA," "nanowire," "nanotube," "optical," "mechanical," "biological") or using "***other***" ***unspecified*** technologies. 26:17-31.

2. **Numerical Representation**. Each execution unit is adapted to operate on either (i) fixed point, logarithmic, or floating-point digital representations of

numbers, (ii) analog representations of numbers such as "charges," "voltages," "various forms of spikes," or "other forms," or (iii) a combination of digital and analog representations. 11:53-56, 14:16-26, 24:47-57.

3. **Operation**. Each execution unit is adapted to execute at least one operation ranging from addition to multiplication to a trigonometric operation or exponentiation. 1:63-66, 11:44-48, 27:31-40.

There are an immense number of ways to combine the above variables, and thus an immense number of different types of execution units the claims cover, including DNA-implemented and nanomechanical-implemented execution units operating on analog representations of numbers to perform trigonometric operations, silicon-implemented execution units operating on analog representations (*e.g.*, pulse densities) to perform multiplication, and execution units implemented using some "***other***" unspecified technology operating on analog representations using some "***other***" unspecified physical characteristic to perform a non-linear operation. Goodin, ¶ 65. And, of course, ***all*** these implementations somehow must perform their operation with the claimed functional performance characteristics.

b. The Claims Specify Functional Performance Characteristics of the "Execution Unit" Genus Rather Than Structural Features Common to Members of That Genus

As shown above, the specification says the claimed "execution unit" can be ***any*** unit "adapted to execute" ***any*** "operation" on a first input signal (in digital and/or

analog representation) to produce an output signal. The only "limits" the claims impose on the "execution unit" are functional performance characteristics (high dynamic range and low precision) similar to the "fuel efficient" characteristic in the *LizardTech* hypothetical.

The independent claims' requirement that the "execution unit" perform an operation on a **high dynamic range** of numbers (*i.e.*, at least as wide as from 1/65,000 through 65,000) was not novel; the '273 patent concedes execution units that performed precise operations on HDR numbers were known. 3:15-18, 4:13-17; Goodin, ¶ 66; Tong (Ex. 1008), 274.

The independent claims' requirement that the "execution unit" perform its operation with **low precision** is recited in terms of the percentage of inputs ("at least X=5%") for which the output of the operation differs, on average ("statistical mean"), by a specific (but unbounded) percentage ("at least Y=0.05%") from an exact mathematical calculation of the same operation, and it too was not novel. Goodin, ¶¶ 67-69. The '273 patent admits low-precision high-dynamic range execution units were known but alleges they simply were considered "not useful." '273 patent, 6:57-7:11; Goodin, ¶ 69.

The "execution unit" is thus characterized as a "***low precision*** high dynamic range (LPHDR) execution unit" (29:66-67) because for at least a certain percentage of calculations the output is at least a certain percent different from the "exact

mathematical" answer. Goodin, ¶ 70. The challenged claims cover any "execution unit adapted to execute" any HDR operation with the recited minimum degree of imprecision. *Id*.

3. The '201 Application's Disclosure Does Not Demonstrate Full Possession of Any Challenged Claim

The '201 Application does not demonstrate that Dr. Bates invented what the challenged claims recite—***all*** types of HDR execution units, no matter how implemented, that can operate on digital and/or analog representations of numbers to perform ***any*** operation imprecisely enough to meet the claimed functional performance characteristics.

As discussed *infra* § V.B.3.a, the application at best provides details about one potential implementation—an execution unit implemented using conventional silicon transistors to perform low-precision arithmetic on digital representations. Even for that conventional implementation, however, the application fails to show possession of a ***claimed*** execution unit because it fails to tie the claimed imprecision level (X and Y percentages) to a specific implementation using conventional digital circuitry; among other things, the application fails to explain how many bits to use for a particular operation on a particular numerical representation (*e.g.*, logarithmic or floating-point) to achieve the claimed (Y) amount of error for the claimed (X) percentage of valid inputs. Goodin, ¶ 88.

But the Board need not even wrestle with the question of whether the '201 Application demonstrates possession of a species of the claimed execution unit implemented using conventional digital circuitry, because even if such possession were established, it would be insufficient to demonstrate "***full*** possession of the claimed subject matter," given that the application manifestly does not demonstrate possession of any of the vast number of ***other*** types of execution units the claims cover. *TurboCare*, 264 F.3d at 1118.

The application explicitly says that whether an execution unit satisfies the required functional performance characteristics "***var[ies] from implementation to implementation***." [0142], [0144];[5] Goodin, ¶ 71. The application is thus candid that the claimed "execution unit" can be any device with any structure that implements the abstract idea of executing operations with low precision. Goodin, ¶ 72. The '201 Application, however, fails to provide ***any*** design details for how to implement numerous of the referenced species of execution units (*e.g.*, a "nanomechanical" implementation, a "DNA" implementation, or an "other [unspecified] technologies" implementation ([0139])), let alone one that is capable of executing ***any*** mathematical operation with the claimed functional performance

[5] Citations in § V.B.3 are to Ex. 1005 unless otherwise indicated.

characteristics. These required details are absent because Dr. Bates could not describe what he did not possess.

In *Ariad*, the *en banc* Federal Circuit held claims lacked written description support because they covered "any compound later actually invented and determined to fall within the claim's functional boundaries—leaving it to the pharmaceutical industry to complete an unfinished invention." 598 F.3d at 1353. That is effectively what Dr. Bates did here. He did little more than describe the known abstract idea that performing imprecise computer operations was beneficial in certain applications. [0020]-[0021]; Goodin, ¶¶ 73-74 (discussing Tong prior-art reference). Dr. Bates then identified numerous specific values for a minimum amount of error (Y) and a minimum percentage of valid inputs (X) resulting in that amount of error, and claimed many combinations of those values across his various patents without establishing criticality for any claimed combination of X and Y values. [0144]. Dr. Bates further claimed ***every*** possible execution unit that would possess the functional performance characteristics specified by particular X and Y values, without remotely demonstrating possession of that massively broad genus of execution units.

The '201 Application's identification of technologies (*e.g.*, "nanomechanical" and "DNA computing" ([0139]) that ***might*** be capable of implementing an execution unit as claimed, depending in some ***unspecified*** way on how the execution unit

would be implemented using those technologies, is insufficient to demonstrate that the inventor actually was in possession of such subgenera, let alone the entire claimed genus which also encompasses execution units implemented in unspecified ways using "other [unspecified] technologies." *Id*. The Federal Circuit has expressly and consistently rejected the "argument that the written description requirement…is necessarily met…[even where] the claim language appears *in ipsis verbis* in the specification." *Enzo Biochem, Inc. v. Gen-Probe Inc.*, 323 F.3d 956, 968 (Fed. Cir. 2002); *Ariad*, 598 F.3d at 1350.

For example, in *Nuvo Pharms. v. Dr. Reddy's Labs.*, 923 F.3d 1368, 1372-73 (Fed. Cir. 2019), the Federal Circuit held claims reciting uncoated acid inhibitors effective to raise gastric pH to at least 3.5 lacked written description support. The patentee's expert had identified, *inter alia*, a passage in the specification explicitly stating that "[t]he composition contains an acid inhibitor present in an amount effective to raise the gastric pH of a patient to at least 3.5," but the Federal Circuit found such disclosure insufficient because the specification "never discusses or explains [the inhibitor's] efficacy." *Id.* at 1379-80. "In light of the fact that the specification provides nothing more than the mere claim that uncoated [inhibitor] might work, even though persons of ordinary skill in the art would not have thought it would work, the specification is fatally flawed." *Id.* at 1381. The '201 Application is similarly flawed because it does nothing more than say certain potential subgenera

of "execution units" (*e.g.*, those implemented using nanomechanical or DNA computing technology) ***might*** somehow possess the claimed low-precision performance characteristics, without describing an execution unit within those subgenera that actually possesses those characteristics.

a. The '201 Application's Description of a Conventional Digital Silicon Transistor-Based Implementation

The LPHDR "execution unit" implementation the '201 Application describes with the most specificity is one using silicon transistor-based circuits that operate on digital representations of numbers.[6] [0035], [0061]-[0062]. That is unsurprising as this was conventional technology that had already been used to implement an LPHDR execution unit. Goodin, ¶ 75 (citing Dockser and Tong).

The '201 Application mentions an execution unit using a floating-point digital number representation having a 10-bit mantissa, 6-bit exponent and 1-bit sign, and characterizes that floating-point execution unit as "represent[ing] values from one millionth up to one million with a precision of about 0.1%." [0035]. Other than that reference, a floating-point execution unit is nowhere else described. Goodin, ¶¶ 76-77. The application does not explain what "precision of about 0.1%" means and

[6] The application also describes a "mixed" implementation using analog and digital representations. [0078]. That implementation, however, is not described as meeting the claimed functional performance characteristics. *Infra* § V.B.3.b(1).

does not tie it to the claimed error (Y) and frequency (X) characteristics. *Id*. Even if "precision of about 0.1%" were considered to describe the claimed error amount characteristic (which is not clear), the application says nothing about the percentage of valid inputs that would have this amount of error in the floating-point execution unit, and thus does not describe a floating-point execution unit with an error frequency of "at least X=5%" as recited in the independent claims. [0035]; Goodin, ¶ 77. No explanation is provided of ***how*** to implement a floating-point unit to ensure that it has the claimed functional performance characteristics. Goodin, ¶ 77.

An execution unit that operates on logarithmic numeric representations is described in more detail. [0035], [0061]-[0074], FIGS. 4-6. The application describes an implementation having "a multiplicative error of approximately 1%" ([0062]), but does not explain what this means and does not tie it to the claimed error (Y) and frequency (X) imprecision characteristics. Goodin, ¶¶ 78-83. Even if this 1% error were considered to support the claimed minimum error (which is not clear), the '201 Application says nothing about the percentage of valid inputs that would have this amount of error and thus does not describe a logarithmic execution unit meeting "at least X=5%" as recited in the independent claims. [0035]; Goodin, ¶ 83.

The '201 Application also describes a software "model" that simulates the logarithmic embodiment using "repeatable" "arithmetic" that "produces errors of up to approximately 1-2% in each operation." [0085]-[0088]; Goodin, ¶ 84. Once

again, the application says nothing about the percentage of valid inputs that would produce the minimum relative error required by each challenged claim. Goodin, ¶ 85. The application reports a "mean score error" from a number of test runs comparing the results of executing certain high-level software programs using this model against the results of performing those same software programs using "high precision" arithmetic, but those results show the error in the high-level ***program's*** results, not the amount of error in an individual ***operation*** as the claims require. [0090]-[0110]; Goodin, ¶ 85. For example, the "mean score error" for the "nearest neighbor" program refers to the error in a "score" produced by the program, where producing the score can involve ***millions*** of individual operations, and the amount of error in any individual operation cannot be discerned from the average error in the final score produced. [0101]-[0110]; Goodin, ¶¶ 86-87.

For the foregoing reasons, Petitioner does not believe the '201 Application describes an execution unit implemented with conventional technology (*i.e.*, silicon transistor-based circuits) and operating on digital representations of numbers that meets any challenged claim. But the Board ***need not decide that issue*** to find that the challenged claims lack written description support in the application. Even if the Board were to find that the application demonstrates possession of such a digital implementation, that would not suffice because the application manifestly does not demonstrate Dr. Bates possessed any of the vast number of ***other*** types of execution

units the claims cover. *AbbVie*, 759 F.3d at 1300. To demonstrate possession of the genus of execution units claimed, the '201 Application must describe either (1) a representative number of species or (2) structural features common to the genus. *Ariad*, 598 F.3d at 1350. The application does neither.

b. The Digital Silicon Transistor-Based Implementation Is Not Representative of the Vast Genus of Execution Units Claimed

For genus claims, the Federal Circuit has set forth factors for evaluating the adequacy of the disclosure, including "the existing knowledge in the particular field, the extent and content of the prior art, the maturity of the science or technology, [and] the predictability of the aspect at issue." *Capon v. Eshhar*, 418 F.3d 1349, 1359 (Fed. Cir. 2005). Applying these factors to the '201 Application's disclosure demonstrates its inadequacies.

(1) The Digital Silicon Transistor-Based Implementation Is Not Representative of Analog Execution Units Implemented in Silicon

The claims encompass silicon-implemented execution units operating on ***analog*** representations of numbers such as "charges, currents, voltages, frequencies, pulse widths, pulse densities, various forms of spikes, or in other forms not characteristic of traditional digital implementations." '273 patent, 14:16-26; *supra* § V.B.2.

Analog implementations rely on "the natural analog physics of transistors or other physical devices instead of using only the digital subset of the device's behavior." [0036]. Analog implementations are more unpredictable than digital implementations and can be non-deterministic (*i.e.*, an analog execution unit may produce different results at different times for the same input value). [0026], [0141]; Goodin, ¶ 89.

Analog computing using silicon circuits was not a nascent technology in 2010. Goodin, ¶ 90. However, the impact of various implementation choices on the ***precision*** of an analog HDR execution unit was unpredictable, and the '201 Application fails to describe any correlation between an analog execution unit's implementation details and its precision. *Id*. The application does not describe what structural features differentiate silicon-implemented analog execution units that meet the claimed functional performance characteristics from those that do not, or how to adjust silicon-implemented analog execution units to meet the claimed imprecision characteristics. Goodin, ¶ 91.

The application identifies a prior-art analog design that is alleged to perform "a range of low precision" computations, but only on a "low dynamic range" of values (not HDR as claimed) and only for relatively simple operations like addition and subtraction. [0076]-[0077]. The application states this prior art design "***suggest[s] the general feasibility***" of an analog implementation ([0077]), but

describes no modification alleged to enable the prior-art analog-only implementation to perform any ***high*** dynamic range operations as claimed, let alone do so with the claimed imprecision. The application also fails to explain how to modify the prior art design in analog only to perform the full range of operations the specification describes, including multiplication operations the application admits the prior art analog system could ***not*** perform ([0076]-[0077]) and more complex trigonometric or exponentiation functions. '273 patent, 1:63-66, 11:44-48, 27:31-40; Goodin, ¶¶ 92-93.

Tellingly, six years after filing the '201 Application, Dr. Bates publicly admitted he was unable to get ***an analog implementation*** to work (Ex. 1022, 5:6-13), underscoring his lack of possession when the application was filed. *Taylor v. Iancu*, 809 F. App'x 816, 820 (Fed. Cir. 2020) (inventor's testimony that prototype was not available until after the filing date and did not contain all claimed features "shows that the specification did not demonstrate possession of the claimed invention but was instead a mere wish or plan for obtaining the claimed invention"); *Nuvo Pharms.*, 923 F.3d at 1381 (inventor testimony can "illuminate[] the absence of critical description").

The '201 Application also mentions a ***mixed*** analog-digital floating-point implementation that uses an analog mantissa and a digital exponent, but merely alleges the analog ***representation*** of the mantissa is "accurate roughly to ***within*** 1%."

[0076]-[0082]. In other words, the analog-represented inputs to the operation are ***at most*** 1% imprecise, but the application does not say whether any input reaches that maximum imprecision or, if so, how often. Goodin, ¶ 94. Having an imprecise input also does not disclose an execution unit as claimed that introduces imprecision in its performance of a mathematical operation and ***produces results*** that differ from an exact mathematical calculation on the input signal by, *e.g.*, "***at least Y=0.05%***" for at least 5% of valid inputs as claimed in the independent claims. Goodin, ¶ 95. Consider an example that imprecisely represents the decimal input 1.00 as 1.01 and the decimal input 2.00 as 1.98. Each of those inputs is 1% imprecise; however, the ***output*** of multiplying those inputs could be perfectly precise—*e.g.*, $1.01 \times 1.98 = 1.9998$—or could have some different percent error—*e.g.*, outputting 2.0 which is 0.01% (not 1%, and not "at least 0.05%" as claimed) different from the exact result of 1.9998. Goodin, ¶ 96.

The '201 Application also discloses "mean score error" results from running high-level software programs using a software approximation designed to simulate the mixed embodiment by simply ***assuming*** it will produce some random amount of error somewhere between 0-1% in each operation ([0087]), but that does not demonstrate an actual analog hardware circuit would do so, and as with the simulation of the logarithmic embodiment (*supra* § V.B.3.a), the "mean score error"

for the high-level program is not the claimed error in an individual operation. [0085]-[0126]; Goodin, ¶¶ 97-98.

The application does not describe ***even one*** species of an analog implementation (whether pure analog or mixed digital/analog) that falls within any challenged claim's scope, let alone support the silicon-implemented analog subgenera's ***full*** scope. Goodin, ¶ 99. Given the unpredictable nature of analog design using even conventional silicon-based technology, a POSA would not have known if a particular analog implementation would possess the claimed functional performance characteristics without physically building and testing it. Goodin, ¶¶ 100-101 (citing Ex. 1059, 1:14-41). The '201 Application provides no guidance on how to design an analog execution unit that would meet the claims other than through "trial-and-error research," which is insufficient to satisfy section 112. *Univ. of Rochester v. G.D. Searle & Co, Inc.*, 358 F.3d 916, 919 (Fed. Cir. 2004). Pointing to the prior art as "suggest[ing]" that a proposed analog implementation might be "general[ly] feasibl[e]" ([0077]), is not enough. *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1350 (Fed. Cir. 2013).

Compounding the problem is the range of physical parameters the '201 Application alleges could be used to represent numbers in an execution unit. [0075], [0162]; *supra* § V.B.2.a. To demonstrate possession of the full subgenus of silicon-implemented analog execution units, the application would need to demonstrate

possession of species of execution units sufficient to represent the entire subgenus that encompasses every one of these physical parameters, yet it discloses none. Additionally, the application alleges that a silicon-implemented analog execution unit as claimed could be based on "other" entirely unspecified physical parameters. [0075]. The '201 Application clearly does not demonstrate that the inventor possessed a silicon-implemented analog execution unit as claimed that operates on some unspecified physical parameter nowhere mentioned in the application.

(2) The Digital Silicon Transistor-Based Implementation Is Not Representative of Execution Units Implemented Using Unpredictable and Nascent Technologies

The claims encompass non-silicon-implemented execution units operating on digital or analog representations of numbers and implemented using nascent and unpredictable technologies such as "nanomechanical and nanoelectronic technologies, chemistry based technologies such as for DNA computing, nanowire and nanotube based technologies, optical technologies, mechanical technologies, biological technologies, and other technologies whether based on transistors or not." '273 patent, 26:17-31; *supra* § V.B.2.

The '201 Application lists these nascent technologies and speculates they "***may***" be used to implement LPHDR execution units that could perform some unspecified mathematical "operation" on digital or analog representations, but provides no description of how an execution unit could be designed using any one

of the nascent technologies (*e.g.*, nanomechanical or DNA computing), let alone a description of what implementation techniques would need to be used to ensure that any such execution unit would possess the challenged claims' low-precision functional performance characteristics. Goodin, ¶¶ 102-103. The reason for this silence is clear: "one cannot describe what one has not conceived." *Fiers*, 984 F.2d at 1171.

That the technologies listed in the '201 Application were nascent and unpredictable is undeniable. Goodin, ¶ 104. For example, nanotechnology involves "creation and use of structures, devices, or systems" of a size "at the level of atoms and molecules." Ex. 1021, 16; Goodin, ¶ 104. Around the time of the alleged invention, POSAs viewed nanotechnology as a futuristic manufacturing technology that might ***someday*** allow for more complex and precise structures; however, no nanotechnology computer or execution unit of the type claimed had been realized. Goodin, ¶ 105. As a 2006 article regarding nanotechnology explained, "the majority of nanoscale scientists and engineers believe it is too early to try to predict the ultimate capabilities of such systems." Ex. 1021, 107. The article described nanotech computing as "visionary engineering," and contrasted it with "conventional engineering" that was "concerned with the design of things that can be built more or less immediately." *Id*. As the article put it succinctly: "[S]howing

that [a structure] can, in principle, exist[] does not tell one how to build it, and these arguments do not yet constitute a research strategy or a research plan." *Id*.

Designing computer circuits using nanotechnology was (and remains) a nascent and unpredictable technology. Goodin, ¶¶ 106-107; Ex. 1047, 36-37 (2010: technology for "[n]anocomputer architectures" "is not yet realized"); Ex. 1048, 3 (2019: material required for nanotube chips "is virtually impossible"). The '201 Application suggests as much when it predicts that the advantages of its execution unit when "fabricated with current state of the art technology" would "persist as fabrication technology continues to improve, even as we ***reach*** nanotechnology or other implementations for digital and analog computing." [0128]. Despite this, the application provides no details concerning nanotechnology-based circuits to suggest the inventor actually possessed a nanotechnology-based execution unit that could perform ***any*** LPHDR operation in 2010 when the application was filed, let alone the full scope of mathematical operations (including non-linear and trigonometric functions) alluded to in the specification with the claimed imprecision. [0006], [0059], [0144].

In addition to nanotechnology, numerous other technologies listed in the '201 Application were nascent and unpredictable, and a POSA would not have known how to implement the claimed execution unit using them. *E.g.*, Ex. 1049, 1 (2015: ***DNA computing*** is "untenably slow"); Ex. 1050 (2013: explaining "no one has made

a [CPU] based on," *e.g.*, "biological computers"); Ex. 1051, 503 (2017: "***Optical computing***…solutions have been elusive."); Goodin, ¶ 108.

The '201 Application's aspirational disclosure reveals the applicant listed numerous implementations he did not possess in an attempt to capitalize on (and monopolize) the future work of others who might someday use the identified nascent technologies to develop an execution unit that happened to operate with the low-precision functional performance characteristics the claims recite. Section 112 prohibits such aspirational claim drafting. *Ariad*, 598 F.3d at 1352. As the application nowhere suggests actual possession of any "execution unit" using the listed nascent technologies (Goodin, ¶ 109), its disclosure cannot provide written description support for a claimed genus encompassing such execution units. *Novozymes*, 723 F.3d at 1350 ("[A POSA] reading the…application would have understood that Novozymes had only predicted that at least some mutations…would yield variants with increased thermostability, not that it possessed or had definitively identified any mutations that would do so.").

(3) Conclusion: The Digital Silicon Transistor-Based Implementation Is Not Representative of the Claimed Genus

A vast number of aspirational species are covered by the claimed genus of all HDR execution units (no matter how implemented) that operate with the claimed amount of minimum imprecision, including numerous subgenera the specification

says are covered but does not actually describe. Thus, even if the Board were to find that a silicon-implemented transistor-based digital implementation meeting the claims was sufficiently described (it was not), that is not remotely representative of the entire genus. Goodin, ¶ 110.

c. The '201 Application Does Not Disclose Structural Features Common to the Claimed Genus

As explained *supra* § V.B.3.a, a disclosure can support a functionally defined genus by describing "structural features common to the members of the genus so that one of skill in the art can 'visualize or recognize' the members of the genus." *Ariad*, 598 F.3d at 1350. The '201 Application does not provide such disclosure. Indeed, the application does not describe the genus using ***any*** structural features. Instead, it characterizes the genus only using functional performance characteristics that specify the precision with which the execution unit operates—any execution unit that operates with such imprecision is within the genus regardless of the structural features used to implement it. Goodin, ¶ 111.

As explained *supra* § V.B.2, the claimed genus encompasses digital and analog implementations that may be implemented using disparate technologies ranging from silicon transistors to nanomechanical or DNA computers with "structural features" that are entirely undisclosed. There is ***nothing*** in the application suggesting there are common structural features among a traditional silicon-based circuit that processes digital representations and nanomechanical and

DNA-based units that operate on analog representations. Goodin, ¶¶ 112-113. Indeed, there are no such common structural features because the genus is not defined by anything structural—the only thing "common" to the genus is that all execution units encompassed thereby must share a functional performance characteristic, *i.e.*, operating with the specified degree of minimum imprecision. *Id*.

C. Enablement: The '201 Application Does Not Enable the Full Scope of Any Challenged Claim

In addition to written description, "the specification must ***enable*** the ***full*** scope of the claimed invention." *Trustees of Boston Univ. v. Everlight Elecs. Co.*, 896 F.3d 1357, 1364 (Fed. Cir. 2018). Enablement "is met where [POSAs], having read the specification, could practice the invention without undue experimentation." *Streck, Inc. v. Res. & Diagnostic Sys.*, 665 F.3d 1269, 1288 (Fed. Cir. 2012) (quotation omitted).

Here, the '201 Application says the claims encompass numerous embodiments for which the specification is devoid of any details (*supra* § V.B.), impermissibly leaving to the public the difficult (if not impossible) task of determining how to implement many of the "execution units" the claims cover (*e.g.*, those using analog numerical representations, nascent technologies and implementing complex non-linear and trigonometric functions). Singular sought broad claims "at the peril of losing any claim that cannot be enabled across its ***full***

scope of coverage." *MagSil Corp. v. Hitachi Global Storage Techs.*, 687 F.3d 1377, 1381 (Fed. Cir. 2012).

While not mandatory, the factors in *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988), may be considered when determining if a disclosure requires undue experimentation such that the claims are not enabled under section 112. As discussed below, those factors indicate that the '201 Application does not enable any challenged claim's full scope.

1. Breadth of the Claims and Nature of the Invention (*Wands* Factors 4 and 8)

As explained *supra* § V.B.2, the challenged claims broadly recite an "execution unit" that can be virtually ***anything*** "adapted to execute" ***any*** mathematical "operation" on an input signal that represents an HDR numerical value (via digital or analog representation) so long as the execution unit possesses the claimed low-precision functional performance characteristics. Goodin, ¶ 114. Those imprecision performance characteristics are recited with no upper limit. *E.g.*, claim 1 ("***at least*** X=5%" and "differs by ***at least*** Y=0.05%.").

Similarly, the nature of the alleged invention is an "execution unit" that can perform arithmetic operations on numerical values of high dynamic range with low precision. '273 patent, 2:11-39. Goodin, ¶ 115. The claimed invention is defined not by any structural aspect of an "execution unit," but solely by its performance characteristics. The functional way in which the specification characterizes the

alleged "invention" underscores the lack of guidance the applicant provided POSAs about how to implement the full scope of that "invention."

2. The State of the Art, POSA's Skill, the Level of Unpredictability, and Quantity of Experimentation (*Wands* Factors 1 and 5-7)

As explained *supra* § V.B.2.a, the '201 Application's laundry list of ***potential*** implementations makes clear the claimed "execution unit" covers, *inter alia*, nanotechnology-based and DNA-based "circuits," operating on analog representations of numbers, which were entirely unpredictable. Goodin, ¶ 116. It would not have been within the POSA's ordinary skill to develop an HDR execution unit that could perform ***any*** mathematical operation using these aspirational technologies, let alone one that could perform complex non-linear or trigonometric functions of the type the specification says are covered by the claims, without undue experimentation. *Id*.

Compounding the complexity, the claims cover analog representations using a wide range of physical characteristics ("charges, currents, voltages, frequencies, pulse widths, pulse densities, various forms of spikes") including "***other forms***" the specification nowhere identifies, and cover non-deterministic implementations that generate different results at different times for the same input. *Supra* § V.B.2 (explaining claim scope). Given that the application must enable the ***full*** scope of a challenged claim, its failure to enable aspirational, complex, non-deterministic,

analog implementations using unstated ("***other***") physical characteristics to represent numbers is fatal.

Even a more conventional implementation that uses a ***silicon*** circuit to operate on analog number representations was unpredictable. *Supra* § V.B.3.b(1); Goodin, ¶ 117. POSAs knew how to develop ***some*** silicon circuits that operated on analog numerical representations, but the specification never explains what implementation decisions would purportedly result in a circuit possessing the claimed imprecision characteristics versus a circuit that would not. Goodin, ¶ 117. The application only states that the existence of prior-art analog silicon circuits "suggest[s] the general feasibility" of creating an "execution unit" with the claimed imprecision characteristics ('201 Application, [0077]), but does not inform a POSA how to actually implement an analog execution unit possessing those characteristics.

To arrive at such an "execution unit," a POSA would have needed to undertake significant experimentation. For example, a POSA would have had to measure electrical characteristics such as charge injection, voltage coupling, and parasitic capacitances to determine whether the required error could be achieved; these characteristics are heavily dependent on physical properties of the silicon circuits that are not easily adjusted. Goodin, ¶ 118; *In re '318 Patent Infringement Litigation*, 583 F.3d 1317, 1327 (Fed. Cir. 2009) ("[T]he specification…does no

more than state a hypothesis and propose testing to determine the accuracy of that hypothesis. That is not sufficient.").

Arriving at an analog circuit within the claims would have impermissibly required a POSA to engage in undue experimentation by iterating through a trial-and-error approach, hoping to find an implementation meeting the particular imprecision values claimed for a massive ("high dynamic") range of inputs. *ALZA Corp. v. Andrx Pharm., LLC*, 603 F.3d 935, 941 (Fed. Cir. 2010) (no enablement where POSAs "would have been required to engage in an iterative, trial-and-error process to practice the claimed invention"). That undue experimentation would be required is demonstrated by the inventor's admission years after the filing that: "I couldn't figure out how to do it in analog." Ex. 1022, 5:6-13.

The challenged claims encompass subject matter that was (and remains) only ***theoretically plausible,*** which is insufficient for enablement. Goodin, ¶ 119. As explained in *Rasmusson v. SmithKline Beecham Corp*., 413 F.3d 1318, 1325 (Fed. Cir. 2005), enablement requires more than a "mere possibility."

3. The Amount of Direction Provided, Including Working Examples (*Wands* Factors 2-3)

The '201 Application lacks direction or working examples for most of the implementations the claims cover. Goodin, ¶ 120.

Even if the application is considered to describe digital floating-point or logarithmic implementations using conventional silicon circuits, it manifestly

provides no guidance or working examples for the numerous other implementations of an "execution unit" the application says the invention encompasses. Goodin, ¶ 121. The application ***lists*** numerous futuristic technologies and alleges they "***may enable***" analog as well as digital "computing processors or other [unspecified] devices" ('201 Application, [0139]) but never explains how to make an "execution unit" as claimed using an analog implementation with these futuristic technologies. POSAs' knowledge cannot save Singular given that a POSA would not have been able to implement the full scope of what the specification alleges the claims cover with little (to no) direction from the specification. Goodin, ¶ 122.

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The foregoing goes well beyond Petitioner's initial burden of demonstrating that Bates-2010 is prior art, which was met by Petitioner simply arguing Bates-2010 is prior art. *Supra* § V.A. If Singular alleges a challenged claim(s) is entitled to a priority date predating Bates-2010, Singular bears the burden of production to cite evidence establishing such entitlement. If Singular fails to meet that burden, Bates-2010 is established as prior art in this proceeding. *Id*.

D. Bates-2010 Renders Obvious Claims 1-70

1. Bates-2010 Is Indisputable Prior Art

As shown *supra* §§ V.A-V.C, no challenged claim is entitled to the '201 Application's 2010 filing date, making Bates-2010 prior art under pre-AIA section

102(b) as the claims are entitled only to the '273 patent's February 17, 2012 filing date.

2. The Board Can Use Bates-2010 to Find the Challenged Claims Unpatentable

The Federal Circuit, its predecessor court, and the Board have made clear that a parent application with an identical disclosure to the challenged patent can anticipate challenged genus claims where the parent discloses a species within the claimed genus but the disclosed species is insufficient to support the challenged claims' full scope under section 112. *Reckitt Benckiser LLC v. Ansell Healthcare Prods.*, IPR2017-00066, Paper 35, 17 (Jan. 30, 2018); *Chester v. Miller*, 906 F.2d 1574, 1577 (Fed. Cir. 1990) ("***no impermissible anomaly or logical inconsistency***" in treating parent application as prior art that anticipates "broader claims" it did not adequately describe); *In re Lukach*, 442 F.2d 967, 969-70 (C.C.P.A. 1971).

Here, because the only concrete implementations of LPHDR execution units in the specification do not teach whether or how they meet the claimed X and Y values (*supra* § V.B.3.a), the specification shared by Bates-2010 and the '273 patent does not disclose an anticipatory species of the claimed execution unit. In such cases, courts have found claims rendered obvious by the parent application. *Santarus, Inc. v. Par Pharm., Inc.*, 694 F.3d 1344, 1350-54 (Fed. Cir. 2012) (affirming finding of obviousness of claims over parent patent even though those

claims were not supported by the patent's identical disclosure under section 112); *In re Van Langenhoven*, 458 F.2d 132, 137 (C.C.P.A. 1972).

Accordingly, Petitioner relies on an obviousness theory below. If Singular can establish that the silicon-implemented transistor-based digital implementation is described in the '201 Application (and thus Bates-2010) in a manner that ties it to the claimed functional performance characteristics X and Y, the below-cited disclosures in Bates-2010 would anticipate the challenged claims and still render them obvious because "anticipation is the epitome of obviousness." *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019)

3. An Obvious Implementation of Bates-2010's Silicon Transistor-Based Execution Unit[7]

Bates-2010 discloses a silicon-implemented execution unit that operates on digital representations of numbers using transistors. [0035], [0061]; FIG. 4; *supra* § V.B.3.a. Bates-2010 says such an implementation can use "floating point arithmetic" with "binary mantissas of no more than 10 bits plus a sign bit and binary exponents of at least 5 bits plus a sign bit" to represent values "with a precision of about 0.1%." [0035], [0162]. In this implementation, the unit operates on numbers

[7] Paragraph citations in §§ V.D.3-V.D.23 are to Bates-2010 unless otherwise indicated.

with dynamic range "from one millionth up to one million" to perform operations including, *e.g.*, "multiply[ing]." [0035].

Bates-2010 does not identify a minimum relative error (Y) produced by the above-described floating-point execution unit for a minimum percentage (X) of inputs, but elsewhere suggests an execution unit (divorced from any specific implementation) can be implemented to produce relative error (Y) of at least 0.05% for at least 5% (X) of possible valid inputs. [0172]. Given this suggestion, POSAs would have understood how to emulate in software the performance of the floating-point execution unit, performing a particular type of operation (*e.g.*, multiplication), to determine whether the disclosed operation that "represent[s] and manipulate[s]" floating-point numbers with 10-bit mantissas would produce this level of imprecision that Bates-2010 suggests execution units can achieve. [0035]; Goodin, ¶¶ 125-127. Based on the software emulation, a POSA would have known how to decrease the number of mantissa bits utilized until the relative error amounts for the fractions of valid inputs suggested in paragraph 172 of Bates-2010 are met, and would have had a reasonable expectation of success in doing so. Goodin, ¶¶ 128-129 (citing Dockser (Ex. 1007), [0002] (floating-point "precision… is defined by the number of bits used to represent the mantissa[;] [t]he more bits in the mantissa, the greater the precision."); Tong (Ex. 1008), 278 ("in an FP [floating-point] unit…, [using] fewer bits reduces precision")).

The silicon-implemented transistor-based digital floating-point execution unit, modified as needed to achieve the performance characteristics Bates-2010's paragraph 172 suggests achieving, and implemented in a computing device in accordance with Bates-2010's suggestion ([0007]), meets each element of the challenged claims as demonstrated below. Goodin, ¶ 129.

4. Claim 1

a. [1A1] A device comprising: at least one first low precision high dynamic range (LPHDR) execution unit

Bates-2010 discloses that "[e]mbodiments of the present invention are directed to a processor or other device,…which includes processing elements designed to perform arithmetic operations…on numerical values of low precision but high dynamic range ('LPHDR arithmetic')." [0007]. It also explicitly claims "devices" including one or more LPHDR execution units. Claims 1-2.

Figure 1 depicts "an example overall design of a SIMD processor." [0009]. Figure 1's SIMD processor, *i.e.*, a "device" as claimed (*e.g.*, [0040]; Goodin, ¶¶ 130-132), includes a control unit 106 and "a collection of many processing elements (PEs) 104" ([0043]), where a PE is one example of a "kind of execution unit" that is an "LPHDR element[]" ([0042]-[0043]). Bates-2010 expressly suggests implementing a "collection" of Bates-2010's silicon-implemented transistor-based digital floating-point execution units in a device such as a SIMD processor. Goodin, ¶¶ 133-134.

b. [1A2] adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,

Bates-2010's floating-point execution unit performs operations like "multiply[ing]" on floating-point representations of numerical "values." [0035]. A POSA would have understood that performing multiplication on an input representation of a first numerical value results in the production of an output signal representing a second numerical value (the product of the multiplication). Goodin, ¶ 135.

Bates-2010 depicts "an example design for a Processing Element" in FIG. 4, where a "processing element[]" (PE) is one example "kind of execution unit." [0012], [0042]-[0043]. The execution unit (PE) receives "input" and produces "output" that both "take the form of electrical signals representing numerical values." [0055]. The input signals provide "local data" on which the PE "operate[s]" to produce "results" providing the output signals. [0055], [0057], [0045] ("the PEs…perform computations…on data stored locally in each PE"), [0048] (Input/Output Unit 108 "get[s] data into and out of" PEs), [0051]; Goodin, ¶¶ 136-139. The "LPHDR operations" performed by a PE include "multiplication." [0059].

A POSA would thus have understood that each PE (example execution unit) within Figure 1's SIMD processor is "adapted to execute a first operation," *e.g.*,

multiplication, "on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value," as claimed. Goodin, ¶ 140.

Claims 1 and 2 of Bates-2010 confirm this implementation. Claims 1-2; Goodin, ¶ 141.

Bates-2010 also depicts in FIG. 6 "an example digital implementation of [an] LPHDR arithmetic unit," which is a component of a PE that "performs LPHDR arithmetic operations" including "LPHDR multiplication." [0014], [0055], [0067]. The arithmetic unit receives "inputs, A 602a and B 602b, and produces an output 602c," which "take the form of electrical signals representing numerical values." [0067]. A POSA would have understood that the claimed "LPHDR execution unit" is broad enough to cover either, or both, of PE 400 and LPHDR arithmetic unit 408 within PE 400. Goodin, ¶¶ 142-144.

c. [1B1] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000

Various "[e]mbodiments" of "LPHDR arithmetic mechanisms" can be included in a PE. [0060]. One embodiment is the above-discussed floating-point embodiment that "represents values from ***one millionth up to one million***," which is "at least as wide as" (indeed wider than) "from 1/65,000 through 65,000" as claimed. [0035]; Goodin, ¶¶ 145-146. Bates-2010 also explicitly suggests operating

on the specifically claimed dynamic range ([0171]), and Bates-2010's claims 1 and 2 provide verbatim disclosure of limitation 1B1. Goodin, ¶ 147.

Implementing each execution unit (PE) within Figure 1's SIMD processor to perform a first operation, *e.g.*, multiplication, on a range of possible valid inputs "at least as wide as from 1/65,000 through 65,000," as claimed, would have been a straightforward implementation given Bates-2010's explicit suggestion to do so. Goodin, ¶ 148.

d. [1B2] for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and

Bates-2010 discloses that:

> for each LPHDR arithmetic element, for at least one operation that the LPHDR unit is capable of performing, for at least fraction F of the possible valid inputs to that operation, for at least one output signal produced by that operation, the statistical mean, over repeated execution, of the numerical values represented by that output signal of the LPHDR unit, when executing that operation on each of those respective inputs, differs by at least E from the result of an exact mathematical calculation of the operation on those same input values…

[0172]. Variables "E" and "F" in Bates-2010 correspond to variables Y and X in limitation 1B2, respectively. Goodin, ¶ 149.

Bates-2010 explicitly suggests implementing an execution unit to produce a relative error amount "E" ("Y" as claimed) of at least 0.05% for a fraction of the possible valid inputs "F" ("X" as claimed) of at least 5%, where the relative error amount is determined by measuring how much "the statistical mean, over repeated execution, of the numerical values represented by that output signal of the LPHDR unit" differs from "the result of an exact mathematical calculation of the operation on those same input values." [0172]; Goodin, ¶ 150. It would have been obvious to a POSA to implement Bates-2010's floating-point execution unit as a deterministic unit as digital circuits conventionally are, such that the claimed "statistical mean, over repeated execution of the first operation on each specific input," is the same as the output of any single execution of that operation on that input, regardless of how many times the execution is repeated. Goodin, ¶ 150; Weiss (Ex. 1011), 1:40-42; Ex. 1022, 5:14-21 (Dr. Bates explaining that digital silicon circuits are "deterministic, which programmers like").

As explained above (§ V.D.3), a POSA would have understood how to implement Bates-2010's floating-point execution unit to achieve the functional performance characteristics explicitly suggested in [0172], which would have resulted in the execution unit meeting limitation 1B2. Goodin, ¶ 151.

For example, for a multiplication operation performed on floating-point input values with 10-bit mantissas as described in Bates-2010 ([0035]), a POSA would have known how to write a computer program to compute, for every possible valid pair of floating-point input values with 10-bit mantissas: (1) the claimed "result of an exact mathematical calculation" of the product of those input values, which is a product including up to a 20-bit mantissa, and (2) the relative error by which the output (when represented using only a 10-bit mantissa as Bates-2010 suggests ([0035])) differs from the exact mathematical calculation. Goodin, ¶ 152. If that computer program demonstrated that the floating-point execution unit using 10-bit mantissas disclosed in Bates-2010 ([0035]) did not meet the relative error E of at least 0.05% for a fraction F of the possible valid inputs of at least 5% as suggested by Bates-2010 in [0172], the POSA would have known that to achieve those desired E and F values the number of mantissa bits should be reduced. Goodin, ¶ 153. A POSA would have known how to reduce the number of mantissa bits and re-run the computer program until a reduced number of mantissa bits was arrived at that yielded the desired E and F values suggested in [0172]. After the POSA determined a number of mantissa bits that produced the desired E (at least 0.05%) and F (at least 5%) values using the computer program, a POSA would have implemented an execution unit using that number of mantissa bits, and such an execution unit would have met limitation [1B2]. Goodin, ¶¶ 153-154.

5. Claims 3, 5, 7-8, 9-10

Claims 3, 7 and 9 recite that "the at least one first LPHDR execution unit" of claim 1 "comprises at least" 10, 100, and 500 "LPHDR execution units," respectively.

Claims 5, 8, and 10 recite that the number of LPHDR execution units in the device of claim 1 exceeds "the non-negative integer number of execution units…adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide" by at least 10, 100, and 500, respectively.

Bates-2010's SIMD processor (FIG. 1) includes a "collection of many" execution units. [0043]. Bates-2010 discloses that "[f]or certain devices… embodied according [to] the present invention, the number of LPHDR arithmetic elements in the device…exceeds the number…of arithmetic elements in the device which are designed to perform high dynamic range arithmetic of traditional precision (that is, floating point arithmetic with a word length of 32 or more bits)," and that "in certain embodiments," the number of LPHDR arithmetic elements exceeds the number of traditional-precision arithmetic elements by over "one hundred," and even by over "five thousand." [0173]. A POSA would have understood Bates-2010's suggestion to implement Figure 1's SIMD processor, *i.e.*, the claimed "device," to include up to over 5,000 more LPHDR execution units than other execution units to apply to all disclosed execution unit embodiments, including the

silicon-implemented transistor-based digital floating-point embodiment. Goodin, ¶¶ 155-158. Alternatively, it would have been obvious to implement a SIMD processor that adopts both Bates-2010's suggestion to include more LPHDR execution units (*e.g.*, up to over 5,000 more), and Bates-2010's suggestion to implement the LPHDR execution units as silicon-implemented transistor-based digital floating-point execution units. Goodin, ¶ 158.

This obvious implementation of Bates-2010's device, following Bates-2010's express suggestion to include up to over "five thousand" more LPHDR execution units (implemented as silicon-implemented transistor-based digital floating-point execution units) than execution units adapted to execute multiplication on 32-bit-wide floating-point numbers, comprises "at least" 10, 100, and 500 more "LPHDR execution units" and thus meets claims 3, 5, 7-8, and 9-10.

6. Claims 2, 4, 6

Claims 2, 4 and 6 recite that the "at least one first LPHDR execution unit" in the device of claims 1, 3, and 5 (respectively) "comprises at least part of an FPGA."

Bates-2010 discloses implementing "embodiments" of its alleged "invention" on "FPGAs," providing POSA with motivation to implement Bates-2010's silicon-implemented transistor-based digital floating-point execution unit to "comprise[] at least part of an FPGA" as claimed, in the device meeting claims 1, 3, and 5. [0040], [0163]-[0165], [0174]; Goodin, ¶¶ 159-160.

7. Claims 11-17

Claims 11-17 depend from claim 8, and recite various minimum percentages for X and Y. Bates-2010 discloses each recited minimum percentage, and explicitly suggests implementing an execution unit that achieves the claimed combinations of minimum percentages. [0172]. Implementing the device of claim 8 with Bates-2010's silicon-implemented transistor-based digital floating-point execution units to achieve the minimum X and Y percentages recited in each dependent claim would have been a straightforward implementation that Bates-2010 explicitly suggests. Goodin, ¶¶ 161-162; *supra* §§ V.D.3-V.D.4 (discussing how POSA would have achieved X and Y percentages); V.D.5 (addressing claim 8).

8. Claim 18

See limitation [1B1] (explaining execution unit operates on a range of inputs from 1/1,000,000 through 1,000,000); § V.D.5 (addressing claim 8). Goodin, ¶ 163.

9. Claim 19

Bates-2010 suggests implementing a device with "only local connections between [execution] units." [0085]. Implementing the device discussed *supra* § V.D.4 (claim 1) with its execution units locally connected, as Bates-2010 explicitly suggests, meets claim 19. Goodin, ¶ 164.

10. Claim 20.

See limitation [1A1] (explaining "device" is a "SIMD" processor); [0040] ("[E]mbodiments may be… a SIMD computer architecture"). Goodin, ¶ 165.

11. Claim 21

Bates-2010 suggests implementing execution units such that each unit has "a small amount of memory local to" it. [0085]. Implementing the device discussed *supra* § V.D.4 (claim 1) with its execution units having memory locally accessible, as Bates-2010 explicitly suggests, meets claim 21. Goodin, ¶ 166.

12. Claims 22-23

Claims 22-23 limit the device of claim 1 by requiring that the device be "implemented on a silicon chip" (claim 22) or "implemented on a silicon chip using digital technology" (claim 23). Bates-2010 suggests implementing digital execution units using silicon fabrication technologies. [0156], [0162], [0165]. Implementing the device discussed *supra* § V.D.4 (claim 1) with Bates-2010's ***silicon***-implemented transistor-based ***digital*** floating-point execution units, as Bates-2010 explicitly suggests, meets claims 22-23. Goodin, ¶ 167.

13. Claim 24

Claim 24 limits the device of claim 1 to one comprising "a digital processor adapted to control the operation" of the LPHDR execution unit. Bates-2010's execution units (including the above-referenced silicon-implemented transistor-based digital floating-point execution unit) receive "instructions" from a "central control unit" ("CU") that can be a "CPU" (central processing unit), *i.e.*, a "digital processor" as claimed. [0024], [0043], [0049]. As seen in Figures 1, 4, and 6, the exemplary SIMD processor's CU sends "control signals 412a-d" to each execution

unit (PE 400 and/or LPHDR arithmetic unit 408) within the device, and "[t]he operation of the PEs is controlled by [the] control signals 412a-d received from the CU 106." [0047], [0057], [0067] ("unit 408 is controlled by control signals 412a-d"). Thus, Bates-2010 teaches a digital processor (the CU implemented as a CPU) that is "adapted to control" the PEs, *i.e.* the LPHDR execution units, as claimed. Goodin, ¶¶ 168-170.

14. Claim 25

Claim 25 combines limitations of claims 9, 19, and 21-23. As explained above with respect to each of those claims, Bates-2010 explicitly suggests implementing a device including silicon-implemented transistor-based digital floating-point execution units and with the recited features. Doing so as arranged in claim 25 would have been a straightforward implementation given Bates-2010's explicit suggestion to do so. Goodin, ¶¶ 171-172.

15. Claim 26

Claim 26 requires the device of claim 1 to be "part of a mobile device." Bates-2010 suggests using a device comprising LPHDR execution units for "mobile computing," *i.e.*, in a "mobile device" as claimed. [0157]. Implementing the device discussed *supra* § V.D.4 (claim 1) as part of a mobile device, as Bates-2010 explicitly suggests, meets claim 26. Goodin, ¶ 173.

16. Claim 27

Claim 27 requires the device of claim 1 to represent "numbers using a logarithmic representation." Bates-2010 suggests using a device comprising LPHDR execution units that represents numbers using "a logarithmic representation" as claimed. [0035]. Implementing the device discussed *supra* § V.D.4 (claim 1) such that its execution unit represented numbers using "logarithmic representation," rather than floating-point, as Bates-2010 explicitly suggests, meets claim 27. Goodin, ¶ 174.

17. Claim 28

See limitation [1B1] (explaining execution unit uses floating-point representation). Goodin, ¶ 175.

18. Claim 29

Claim 29 limits the device of claim 1 to one comprising "input means for receiving data representing an input image; and wherein the input image includes the first input signal." Figure 1's exemplary SIMD device includes an "input/output unit (IOU)" that gets "data into and out of" the device. [0043], [0048]; FIG. 1. If an "input/output unit (IOU)" conveys a non-generic structure, then it discloses the "input means" recited in claim 29 as it is the element the '273 specification identifies as performing the function of "receiving data." '273 patent, 9:6-16; FIG. 1. Goodin, ¶¶ 176-177.

Bates-2010 further discloses using a device comprising LPHDR execution units to perform deblurring of image data, which a POSA would have known involves receiving data representing an input image including the first input signal. [0148]-[0154]; Goodin, ¶ 178. A POSA would have thus understood Bates-2010 to suggest implementing the device discussed *supra* § V.D.4 (claim 1) such that it "comprises input means for receiving data representing an input image; and wherein the input image includes the first input signal" as claimed. Goodin, ¶ 179.

19. Claim 30

Claim 30 requires the device of claim 29 to be "part of a mobile device." Implementing the device discussed *supra* § V.D.18 (claim 29) as part of a "mobile device," as Bates-2010 explicitly suggests [0157], meets claim 30. Goodin, ¶ 180; *supra* § V.D.15 (discussing "mobile device" limitation).

20. Claim 31

Claim 31 requires the device of claim 29 to be "adapted to deblur the input image." Implementing the device discussed *supra* § V.D.19 (claim 29) to be adapted to "deblur the input image," as Bates-2010 explicitly suggests [0148]-[0154], meets claim 30. Goodin, ¶ 181; § V.D.18 (discussing "deblurring").

21. Claim 32

Claim 32 requires the device of claim 1 to be "adapted to perform nearest neighbor search." Bates-2010 suggests using a device comprising LPHDR execution units to "find[] nearest neighbors." [0090]-[0147]. Implementing the

device discussed *supra* § V.D.4 (claim 1) to perform nearest neighbor searching, as Bates-2010 explicitly suggests, meets claim 32. Goodin, ¶ 182.

22. Claims 36-67

In independent claim 36, limitations [36A1]-[36B2] are identical to [1A1]-[1B2], and are met for the reasons discussed *supra* § V.D.4 (claim 1). [36C] is identical to claim 5, except [36C] is broader by omitting the "by at least ten" recited in claim 5; thus [36C] is met for the reasons discussed *supra* § V.D.5 (claim 5). Goodin, ¶ 183.

Claims 37-67 depend from claim 36, but otherwise are identical to claims 2-32, respectively, which depend from claim 1. The limitations recited in claims 37-67 are thus met for the reasons discussed *supra* §§ V.D.5-V.D.21 (claims 2-32). Goodin, ¶ 184.

23. Claims 33-35 and 68-70.

Independent claims 33 and 68 both recite a "device comprising a computer processor and a computer-readable memory storing computer program instructions, wherein the computer program instructions are executable by the processor to emulate a second device," where the "second device" in claim 33 is identical to the "device" of claim 1, and the "second device" in claim 68 is identical to the "device" of claim 36. Goodin ¶¶ 185-186.

Bates-2010 discloses that "embodiments…may be implemented using" a "conventional" computer "programmed with software," *e.g.*, "a software emulator," "to perform the LPHDR operations disclosed herein." [0165]. Given this teaching, a POSA would have had reason to utilize a computer device comprising a processor and computer-readable memory storing computer program instructions (software) to emulate Figure 1's SIMD processor implemented using Bates-2010's silicon transistor-based digital floating-point LPHDR execution unit(s) that meets claims 1 and 36. Goodin, ¶¶ 187-188.

The device being emulated meets the additional limitations of claims 34-35 and 69-70) for the reasons it does *supra* § V.D.5 concerning claim 3 (reciting identical limitations to claims 34 and 69) and claim 5 (reciting identical limitations to claims 35 and 70). Goodin, ¶¶ 189-190.

VI. NO BASIS EXISTS FOR DISCRETIONARY DENIAL

A. Section 314(a): Parallel Litigation Does Not Weigh Against Institution

Singular served Petitioner with a complaint on December 20, 2019, and subsequently amended that complaint on March 20, 2020 (Ex. 1032). Petitioner moved to dismiss the amended complaint, which was denied. Exs. 1034, 1036.

Petitioner filed this Petition expeditiously, roughly four months after denial of its motion to dismiss, two months after receiving Singular's infringement contentions, and contemporaneously with serving preliminary invalidity

contentions. Exs. 1033, 1037-1038. *HP Inc. v. Neodron Ltd.*, IPR2020-00459, Paper 17, 40 (Sept. 14, 2020) (instituting trial where petitioner "acted diligently" in filing petitions "approximately two months after" infringement contentions and before invalidity contentions); *IBM Corp. v. Trusted Knight Corp.*, IPR2020-00323, Paper 15, 12 (July 10, 2020) (instituting trial where petition filed "soon after" invalidity contentions); *Apple Inc. v. Parus Holdings, Inc.*, IPR2020-00687, Paper 9, 16 (Sept. 23, 2020) (instituting trial where petition filed "shortly after…preliminary invalidity contentions").

The factors in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential) ("*Fintiv*") weigh against discretionary denial.

1. Factor-1: Stay Potential

If instituted, Petitioner will move to stay the litigation, but without "specific evidence" of how the Court will rule this factor is neutral. *Sand Revolution II v. Continental Intermodal Group–Trucking*, IPR2019-01393, Paper 24, 7 (June 16, 2020) (informative).

2. Factor-2: Trial Timing

No trial date has been set, Ex. 1038, which "***weighs heavily against denying institution***." *IBM*, IPR2020-00323, Paper 15, 11. The district court was clear: "this case is…very far away from trial." Ex. 1039, 5:4-7.

The impact of the "global pandemic on court congestion and trial dates is likely to add delay." *Google LLC v. Uniloc 2017 LLC*, IPR2020-00479, Paper 10, 12 (Aug. 13, 2020). Civil jury trials in the District of Massachusetts are continued pending further order, Ex. 1040, and "it may be some time before [the court is] even in a position ***to think about scheduling*** a trial…," Ex. 1039, 5:4-7.

3. Factor-3: Litigation Investment

The parties have not made significant investment related to section 102 or 103 issues as Petitioner has only served its preliminary invalidity contentions (contemporaneous with this filing), and expert reports will not be exchanged until well after an institution decision is due. Ex. 1038. Factor-3 thus weighs against institution denial. *Apple*, IPR2020-00687, Paper 9, 17-19 (factor-3 weighs against denial where expert discovery "has yet to take place"); *Sand Revolution*, IPR2019-01393, Paper 24, 10-11 (similar).

Fact discovery is also in its infancy with minimal discovery and no depositions. *HP*, IPR2020-00459, Paper 17, 40 ("fact discovery in its infancy" weights against denial); *NVIDIA Corp. v. Invensas Corp.*, IPR2020-00602, Paper 11, 27 (Sept. 3, 2020) (factor-3 weighs against denial where "significant work remains"). Moreover, as explained above, Petitioner filed this petition diligently, which "mitigates against" any investment in the litigation. *HP*, IPR2020-00459,

Paper 17, 40; *IBM*, IPR2020-00323, Paper 15, 12; *Apple*, IPR2020-00687, Paper 9, 16.

4. Factor-4: Overlap of Issues

Although specific validity issues to be raised in the litigation are largely unknown given its early stages, the Board nonetheless will decide many issues that do not overlap with litigation issues because Petitioner challenges 69 unasserted claims. *Apple, Inc. v. Maxell, Ltd.*, IPR2020-00200, Paper 11, 17 (July 15, 2020) (challenging unasserted claims weighs in favor of institution).

Failure to consider patentability of the unasserted claims would prejudice Petitioner who would be barred from challenging those additional claims in a future IPR should Singular later assert those claims in the pending litigation (or some future litigation). Singular originally asserted four claims against Petitioner (Ex. 1032, ¶ 87), subsequently provided infringement contentions for only one of those four (Ex. 1037), and has expressly reserved the right to re-assert the previously-asserted claims and/or newly assert additional claims (Ex. 1041, 2).

5. Factor-5: Petitioner Is the Litigation Defendant

Petitioner is the defendant, but factor-5 weighs against denial because the Board is likely to reach a final decision before the district court trial. *Supra* § VI.A.2; *Google*, IPR2020-00479, Paper 10, 18.

6. Factor-6: Other Circumstances, Including Merits

This Petition shows the challenged claims are demonstrably unpatentable, which weighs against denial of institution. *Fintiv*, 14–16.

B. Section 325(d): The Petition Presents Art and Arguments Not Previously Considered

The Office has not previously considered the petition's priority-based challenged. Even if the Office had considered any challenged claim's priority date, this petition demonstrates the Office materially erred in affording the claims a priority date earlier than February 17, 2012. Discretionary denial under section 325(d) is not proper. *Advanced Bionics v. MED-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 8-9 (Feb. 13, 2020) (precedential).

VII. CONCLUSION

The Board should institute review and cancel claims 1-70.

Dated: November 6, 2020

Respectfully submitted,
Google LLC

By /Elisabeth Hunt/
Elisabeth A. Hunt, Reg. No. 67,336
WOLF GREENFIELD & SACKS, P.C.

VIII. APPENDIX: CLAIM LISTING

The following claim listing assigns element labels (*e.g.*, [1PRE], [1A], etc.) to certain claims for clarity.

Claim 1
[1A1] A device: comprising at least one first low precision high dynamic range (LPHDR) execution unit
[1A2] adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,
[1B1] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000 and
[1B2] for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.
Claim 2
The device of claim 1, wherein the at least one first LPHDR execution unit comprises at least part of an FPGA
Claim 3
The device of claim 1, wherein the at least one first LPHDR execution unit comprises at least ten LPHDR execution units.
Claim 4
The device of claim 3, wherein the at least one first LPHDR execution unit comprises at least part of an FPGA.
Claim 5
The device of claim 1, wherein the number of LPHDR execution units in the device exceeds by at least ten the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.
Claim 6
The device of claim 5, wherein the at least one first LPHDR execution unit comprises at least part of an FPGA.

Claim 7
The device of claim 1, wherein the at least one first LPHDR execution unit comprises at least one hundred LPHDR execution units.
Claim 8
The device of claim 1, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.
Claim 9
The device of claim 1, wherein the at least one first LPHDR execution unit comprises at least five hundred LPHDR execution units.
Claim 10
The device of claim 1, wherein the number of LPHDR execution units in the device exceeds by at least five hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.
Claim 11
The device of claim 8, wherein X=10%.
Claim 12
The device of claim 8, wherein Y=0.1%.
Claim 13
The device of claim 8, wherein Y=0.15%.
Claim 14
The device of claim 8, wherein Y=0.2%.
Claim 15
The device of claim 8, wherein X=10% and wherein Y=0.1%.
Claim 16
The device of claim 8, wherein X=10% and wherein Y=0.15%.
Claim 17
The device of claim 8, wherein X=10% and wherein Y=0.2%.
Claim 18
The device of claim 8, wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000.
Claim 19
The device of claim 1, wherein the at least one first LPHDR execution unit comprises a plurality of locally connected LPHDR execution units.
Claim 20
The device of claim 1, wherein the device has a SIMD architecture.

Claim 21
The device of claim 1, wherein the device includes memory locally accessible to the at least one first LPHDR execution unit.
Claim 22
The device of claim 1, wherein the device is implemented on a silicon chip.
Claim 23
The device of claim 1, wherein the device is implemented on a silicon chip using digital technology.
Claim 24
The device of claim 1, wherein the device further comprises a digital processor adapted to control the operation of the at least one first LPHDR execution unit.
Claim 25
The device of claim 1, wherein the at least one LPHDR execution unit comprises at least five hundred locally connected LPHDR execution units, wherein the device includes memory locally accessible to at least one of the LPHDR execution units, and wherein the device is implemented on a silicon chip using digital technology.
Claim 26
The device of claim 1, wherein the device is part of a mobile device.
Claim 27
The device of claim 1, wherein the at least one first LPHDR execution unit represents numbers using a logarithmic representation.
Claim 28
The device of claim 1, wherein the at least one first LPHDR execution unit represents numbers using a floating point representation.
Claim 29
The device of claim 1: wherein the device further comprises input means for receiving data representing an input image; and wherein the input image includes the first input signal.
Claim 30
The device of claim 29, wherein the device is part of a mobile device.
Claim 31
The device of claim 29, wherein the device is adapted to deblur the input image.
Claim 32
The device of claim 1, wherein the device is adapted to perform nearest neighbor search.

Claim 33
[33A1] A device comprising a computer processor and a computer-readable memory storing computer program instructions, wherein the computer program instructions are executable by the processor to emulate a second device comprising: at least one first low precision high-dynamic range (LPHDR) execution unit
[33A2] adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value;
[33B1] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000 and
[33B2] for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.
Claim 34
The device of claim 33, wherein the at least one first LPHDR execution unit comprises at least ten LPHDR execution units.
Claim 35
The device of claim 33, wherein the number of LPHDR execution units in the second device exceeds by at least ten the non-negative integer number of execution units in the second device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

Claim 36
[36A1] A device: comprising at least one first low precision high-dynamic range (LPHDR) execution unit
[36A2] adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,
[36B1] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000 and
[36B2] for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;
[36C] wherein the number of LPHDR execution units in the device exceeds the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.
Claim 37
The device of claim 36, wherein the at least one first LPHDR execution unit comprises at least part of an FPGA.
Claim 38
The device of claim 36, wherein the at least one first LPHDR execution unit comprises at least ten LPHDR execution units.
Claim 39
The device of claim 38, wherein the at least one first LPHDR execution unit comprises at least part of an FPGA.
Claim 40
The device of claim 36, wherein the number of LPHDR execution units in the device exceeds by at least ten the non -negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

Claim 41
The device of claim 40, wherein the at least one first LPHDR execution unit comprises at least part of an FPGA.
Claim 42
The device of claim 36, wherein the at least one first LPHDR execution unit comprises at least one hundred LPHDR execution units.
Claim 43
The device of claim 36, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.
Claim 44
The device of claim 36, wherein the at least one first LPHDR execution unit comprises at least five hundred LPHDR execution units.
Claim 45
The device of claim 36, wherein the number of LPHDR execution units in the device exceeds by at least five hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.
Claim 46
The device of claim 43, wherein X=10%.
Claim 47
The device of claim 43, wherein Y=0.1%.
Claim 48
The device of claim 43, wherein Y=0.15%.
Claim 49
The device of claim 43, wherein Y=0.2%.
Claim 50
The device of claim 43, wherein X=10% and wherein Y=0.1%.
Claim 51
The device of claim 43, wherein X=10% and wherein Y=0.15%.
Claim 52
The device of claim 43, wherein X=10% and wherein Y=0.2%.
Claim 53
The device of claim 43, wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000.
Claim 54
The device of claim 36, wherein the at least one first LPHDR execution unit comprises a plurality of locally connected LPHDR execution units.

Claim 55
The device of claim 36, wherein the device has a SIMD architecture.
Claim 56
The device of claim 36, wherein the device includes memory locally accessible to the at least one first LPHDR execution unit.
Claim 57
The device of claim 36, wherein the device is implemented on a silicon chip.
Claim 58
The device of claim 36, wherein the device is implemented on a silicon chip using digital technology.
Claim 59
The device of claim 36, wherein the device further comprises a digital processor adapted to control the operation of the at least one first LPHDR execution unit.
Claim 60
The device of claim 36, wherein the at least one LPHDR execution unit comprises at least five hundred locally connected LPHDR execution units, wherein the device includes memory locally accessible to at least one of the LPHDR execution units, and wherein the device is implemented on a silicon chip using digital technology.
Claim 61
The device of claim 36, wherein the device is part of a mobile device.
Claim 62
The device of claim 36, wherein the at least one first LPHDR execution unit represents numbers using a logarithmic representation
Claim 63
The device of claim 36, wherein the at least one first LPHDR execution unit represents numbers using a floating point representation.
Claim 64
The device of claim 36: wherein the device further comprises input means for receiving data representing an input image; and wherein the input image includes the first input signal.
Claim 65
The device of claim 64, wherein the device is part of a mobile device.
Claim 66
The device of claim 64, wherein the device is adapted to deblur the input image.
Claim 67
The device of claim 36, wherein the device is adapted to perform nearest neighbor search.

Claim 68
[68A1] A device comprising a computer processor and a computer-readable memory storing computer program instructions, wherein the computer program instructions are executable by the processor to emulate a second device comprising: at least one first low precision high-dynamic range (LPHDR) execution unit
[68A2] adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,
[68B1] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000 and
[68B2] for at least 5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least 5% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least 0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;
[68C] wherein the number of LPHDR execution units in the second device exceeds the non-negative integer number of execution units in the second device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.
Claim 69
The device of claim 68, wherein the at least one first LPHDR execution unit comprises at least ten LPHDR execution units.
Claim 70
The device of claim 68, wherein the number of LPHDR execution units in the second device exceeds by at least ten the non-negative integer number of execution units in the second device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (e)(4)

I certify that on November 6, 2020, I will cause a copy of the foregoing document, including any exhibits or appendices filed therewith, to be served via Overnight FedEx at the following correspondence address of record for the patent:

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

Date: November 6, 2020

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,968 words excluding a table of contents, a table of authorities, Mandatory Notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: November 6, 2020

/Alexandra H. Kime/
Alexandra H. Kime
Paralegal
WOLF, GREENFIELD & SACKS, P.C.